



# SPP2301

## P-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPP2301 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

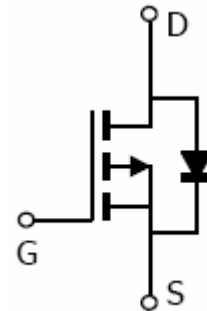
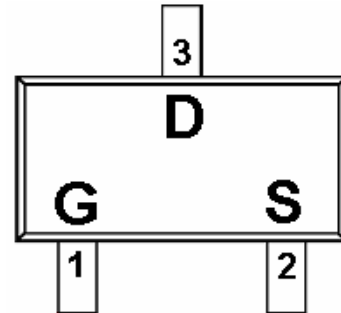
### FEATURES

- ◆ -20V/-2.8A, $R_{DS(ON)}=120m\Omega@V_{GS}=-4.5V$
- ◆ -20V/-2.0A, $R_{DS(ON)}=170m\Omega@V_{GS}=-2.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23-3L package design

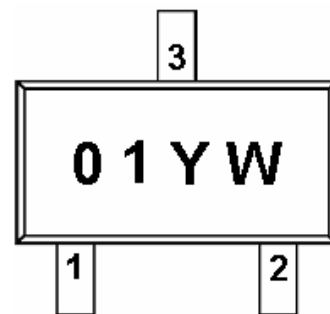
### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### PIN CONFIGURATION(SOT-23-3L)



### PART MARKING



Y : Year Code  
W : Week Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2301S23RG	SOT-23-3L	01YW

Week Code : A ~ Z ( 1 ~ 26 ) ; a ~ z ( 27 ~ 52 )

SPP2301S23RG : Tape Reel ; Pb – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25 Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	-20	V	
Gate –Source Voltage	V <sub>GSS</sub>	±12	V	
Continuous Drain Current(T <sub>J</sub> =150 )	I <sub>D</sub>	T <sub>A</sub> =25	-2.5	A
		T <sub>A</sub> =70	-1.5	
Pulsed Drain Current	I <sub>DM</sub>	-10	A	
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	-1.6	A	
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25	1.25	W
		T <sub>A</sub> =70	0.8	
Operating Junction Temperature	T <sub>J</sub>	150		
Storage Temperature Range	T <sub>STG</sub>	-55/150		
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	120	/W	



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### ELECTRICAL CHARACTERISTICS

( $T_A=25$  Unless otherwise noted)

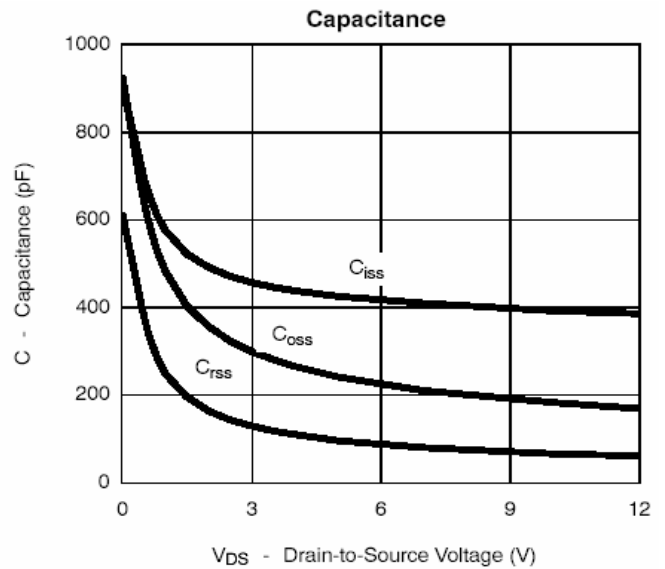
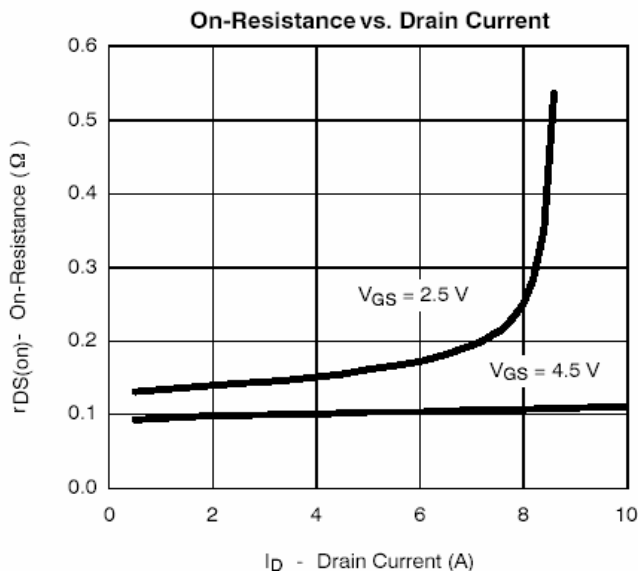
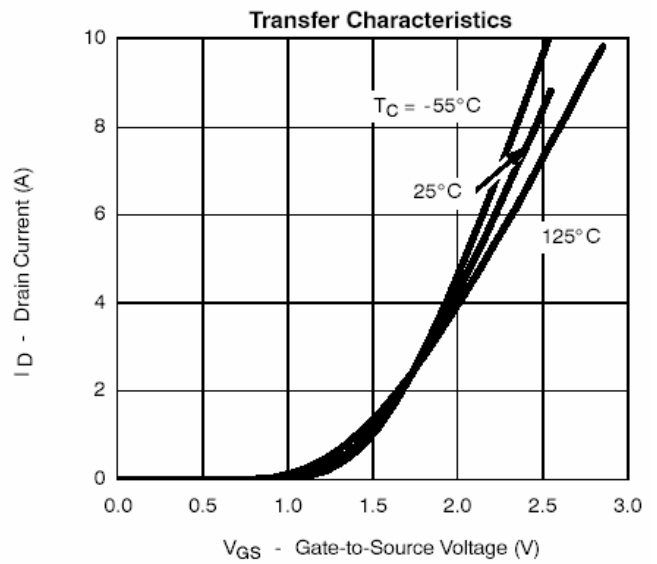
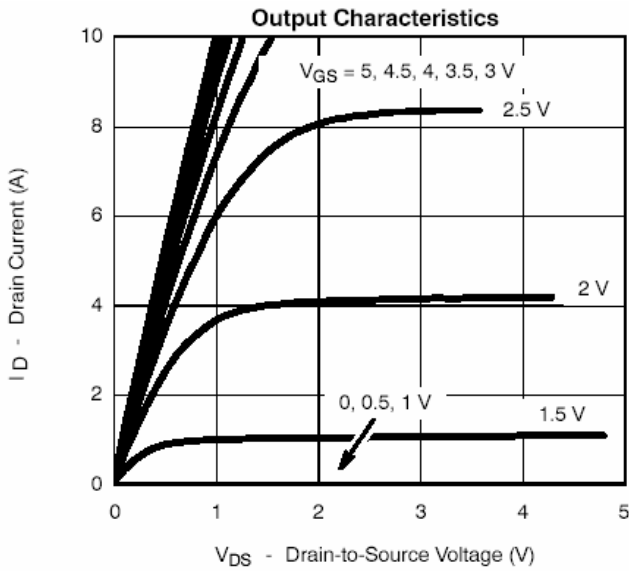
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.45		-1.5	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-20V, V_{GS}=0V$			-1	uA
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=-5V, V_{GS}=-4.5V$	-6			A
		$V_{DS}=-5V, V_{GS}=-2.5V$	-3			
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-2.8A$		0.095	0.12	$\Omega$
		$V_{GS}=-2.5V, I_D=-2.0A$		0.150	0.17	
Forward Transconductance	$g_{fs}$	$V_{DS}=-5V, I_D=-2.8A$		6.5		S
Diode Forward Voltage	$V_{SD}$	$I_S=-1.6A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-6V, V_{GS}=-4.5V$ $I_D=-2.8A$		5.8	10	nC
Gate-Source Charge	$Q_{gs}$			0.85		
Gate-Drain Charge	$Q_{gd}$			1.7		
Input Capacitance	$C_{iss}$	$V_{DS}=-6V, V_{GS}=0V$ $f=1MHz$		415		pF
Output Capacitance	$C_{oss}$			223		
Reverse Transfer Capacitance	$C_{rss}$			87		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-6V, R_L=6\Omega$ $I_D=-1.0A, V_{GEN}=-4.5V$ $R_G=6\Omega$		13	25	ns
	$t_r$			36	60	
Turn-Off Time	$t_{d(off)}$			42	70	
	$t_f$			34	60	



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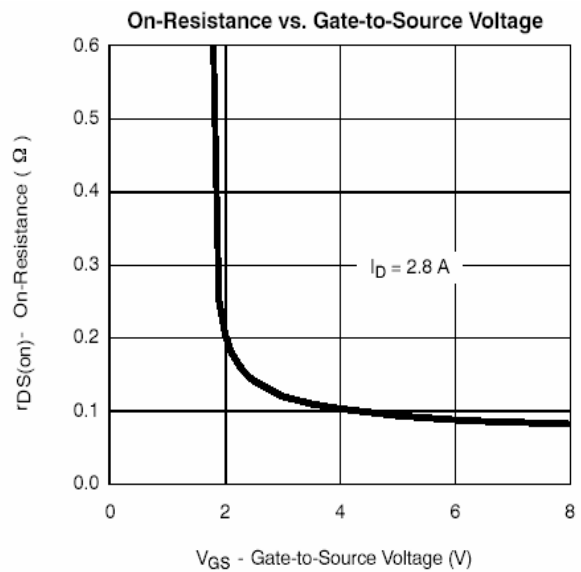
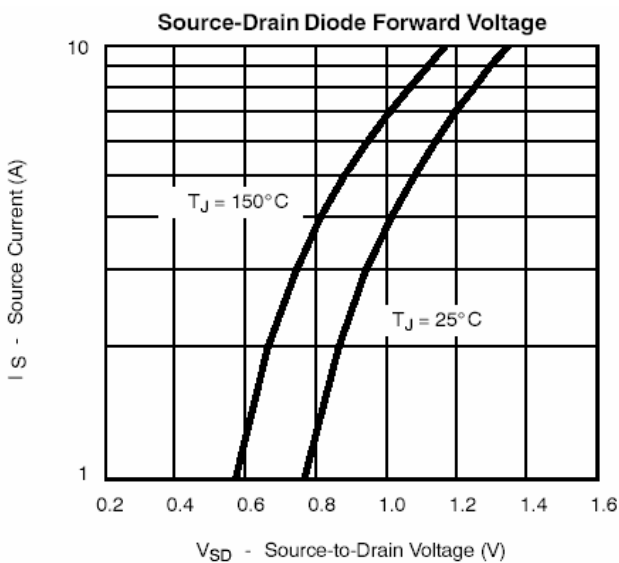
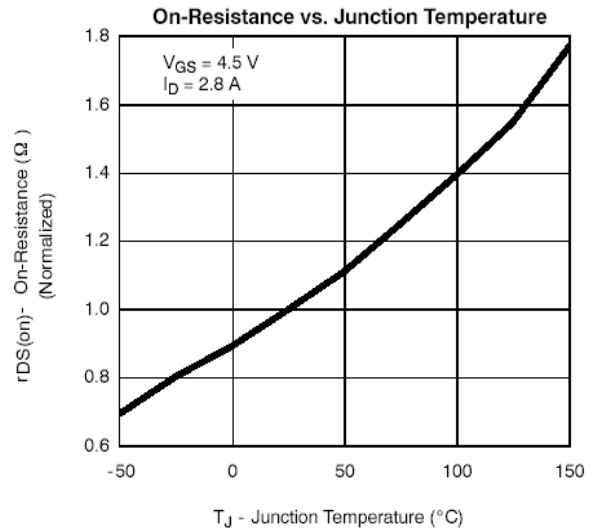
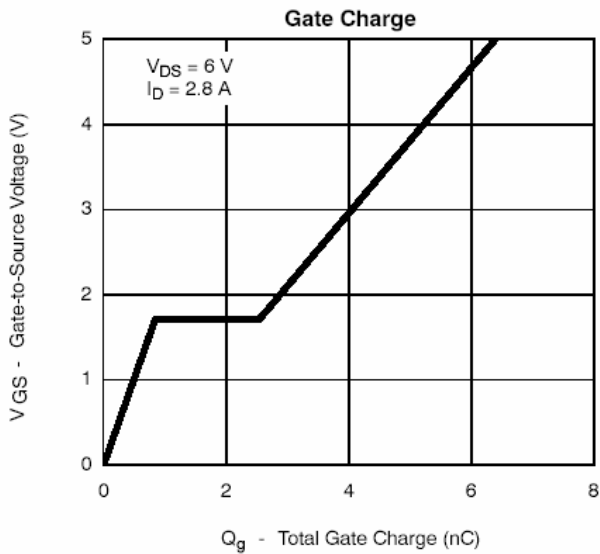
### TYPICAL CHARACTERISTICS





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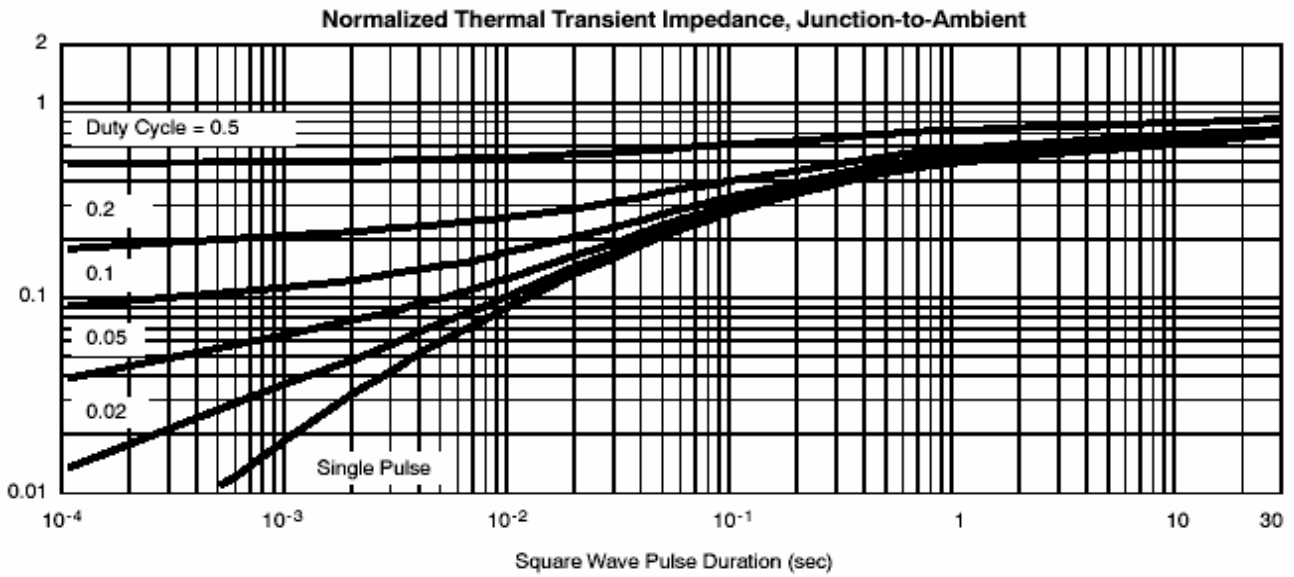
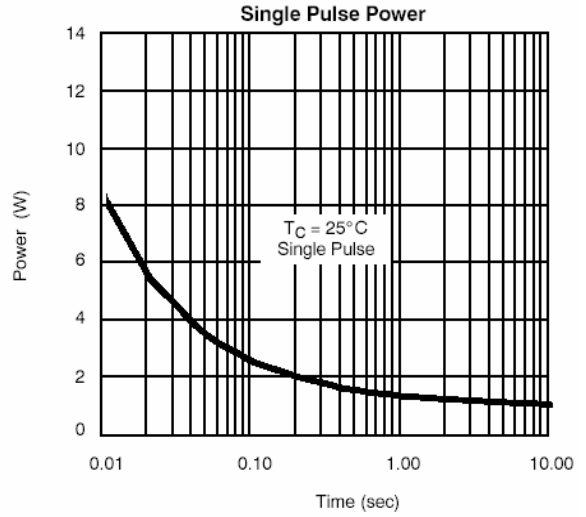
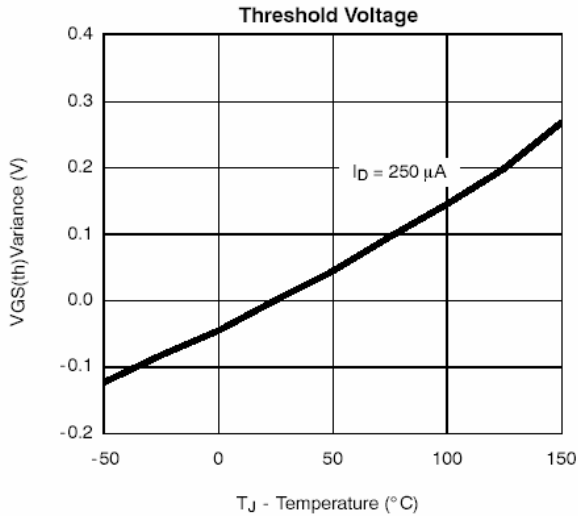
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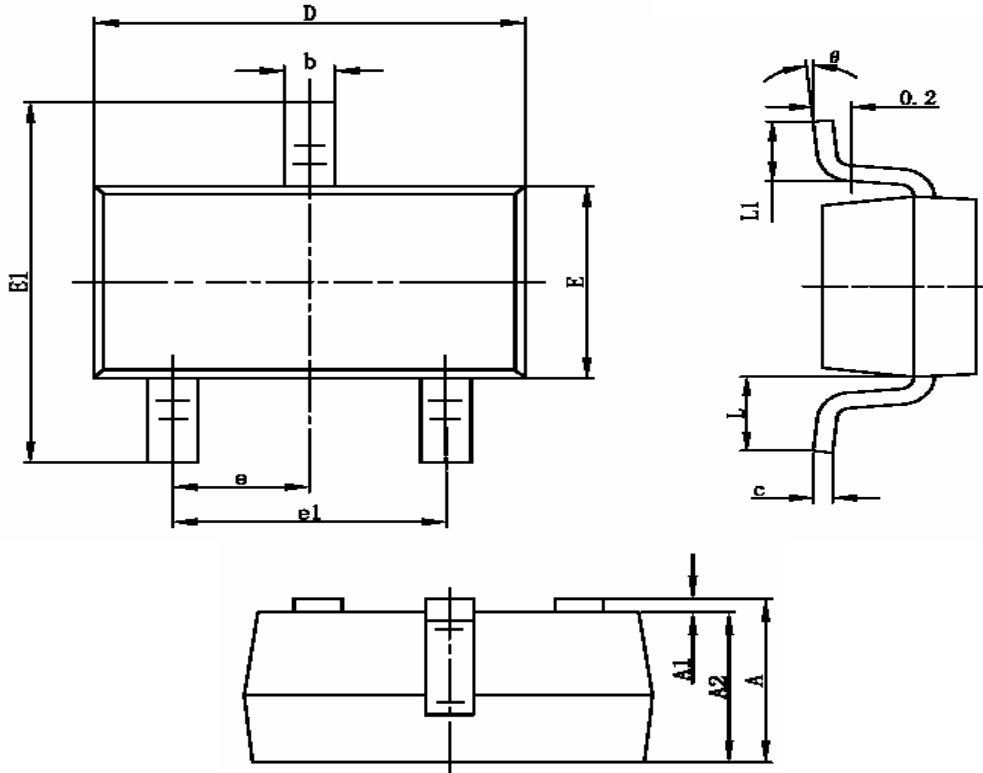




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### SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°



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